ABSTRACT OF THE DISCLOSURE

A memory cell array is of a hierarchical bit line scheme in which cross-point memory cells that exhibit a magnetoresistive effect are laid out in a matrix, and a read bit line to be used in a data read mode is constituted by a main bit line and a sub bit line. A column select circuit selects a main bit line and connects it to a sense amplifier. A row select circuit selects a word line for each cell unit, and in read operation, sets, in a floating state, word lines to which unselected memory cells connected to the sub bit line to which a selected memory cell is connected are connected, and sets the remaining word lines connected to sub bit lines which do not include the selected memory cell to a potential substantially equal to the main bit line.